

TITLE OF THE INVENTION

MIS Transistor and Method of Fabricating the Same

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates to a MIS transistor widely employed for an electronic circuit such as a semiconductor integrated circuit and a method of fabricating the same, and more particularly, it relates to a method of fabricating a MIS transistor through a salicide process employing a refractory metal silicide film for attaining a high speed and high reliability.

10 Description of the Background Art

 An exemplary salicide (self-aligned silicide) process for forming a general refractory silicide film is described with reference to Figs. 47 to 50.

 First, a well 1a, isolation oxide films 2, and an impurity layer 3 for controlling a threshold voltage are formed on a silicon substrate 1. Thereafter a silicon oxide
15 film 4 of 6.5 nm in thickness, for example, is formed on the silicon substrate 1, and a polycrystalline silicon layer for defining a gate electrode is deposited on the oxide film 4 in a thickness of 200 nm. An impurity is added to this polycrystalline silicon layer, which in turn is patterned by a photolithographic step and thereafter anisotropically etched for forming a gate electrode 5.

20 Then, LDD (lightly doped drain) layers 6 which are also referred to as extension layers are formed, and thereafter an oxide film is deposited by CVD (chemical vapor deposition). This oxide film is etched back by reactive ion etching (hereinafter referred to as RIE), for forming side walls 7 consisting of silicon oxide on right and left sides of the gate electrode 5.

25 Then, high-concentration source/drain layers 8 are formed by high-

concentration ion implantation, and thereafter heat treatment is performed for activation. Fig. 47 is a sectional view showing a state after completion of the activation.

Then, the salicide process is carried out.

5 In the salicide process, a surface of the silicon substrate 1 is first cleaned by proper pretreatment, and thereafter a metal film 9 is deposited on the structure shown in Fig. 47 (see Fig. 48).

10 Then, this structure is heated under a proper atmosphere for forming silicide films 10 by the silicon substrate 1 and the polycrystalline silicon forming the gate electrode 5 (see Fig. 49). The composition of these silicide films 10 is expressed as $MSix$, assuming that M represents a metal element forming the metal film 9, for example, where x represents the ratio of silicon atoms to the metal atoms. In this case, short-time heat treatment (rapid thermal annealing) is generally performed through a lamp annealing furnace. The heat treatment which is performed through
15 the lamp annealing furnace immediately after deposition of the metal film 9 is hereafter referred to as first RTA.

At this time, no silicide reaction takes place on upper portions of the isolation oxide films 2 and the side walls 7 due to absence of silicon, and the unreacted metal film 9 remains at least on these upper portions (see Fig. 49). Then, the metal
20 film 9 still containing the unreacted metal M etc. is selectively removed while leaving the silicide films 10 formed by the reacted silicide $MSix$ (see Fig. 50). Basically, the salicide process is ended in the aforementioned step.

However, when the silicide films formed through the aforementioned process are made of titanium silicide $TiSix$, for example, further heat treatment is performed
25 at a high temperature or over a long time for forming titanium silicide films of

TiSi₂ having a different composition or structure, since the electric properties of titanium silicide TiSix are insufficient. Also in case of changing the composition or structure of titanium silicide, short-time heat treatment is generally performed through a lamp annealing furnace. The short-time heat treatment employed for changing the composition or structure of such silicide films is hereinafter referred to as second RTA. Due to the silicide process employing the aforementioned steps, an electrode can advantageously be formed selectively only on a region exposing a silicon surface on the silicon substrate 1.

In recent years, on the other hand, integrated circuits including MIS transistors are implemented with higher density of integration such that the gate length of a planar MOS transistor which is a kind of MIS transistor is refined and side wall widths are also refined in response thereto, for example. However, the conventional MIS transistor fabricated through the silicide process has the aforementioned structure and the silicide film formed on the gate electrode further grows onto the side walls. Due to the small gate length, therefore, the silicide film growing from the gate electrode is disadvantageously connected with those on the source/drain layers if things come to the worst, to result in short-circuiting across the gate electrode and the source/drain layers and deterioration of the yield. Fig. 51 is a sectional view showing a region AR1, enclosed with dotted lines in Fig. 50, in an enlarged manner for illustrating extreme growth of the silicide film. If the diffusion species employed for forming the silicide films is prepared from silicon, short-circuiting is readily caused by creeping of silicide in case of titanium silicide TiSi₂, for example.

Due to the aforementioned structure of the conventional MIS transistor fabricated through the silicide process, further, phase transition from a C49 phase

to a C54 phase hardly takes place in the crystal structure even by second RTA in case of titanium silicide TiSi_2 when the gate length or a silicide wiring width is refined to below $0.5\ \mu\text{m}$, resulting in such a problem that the sheet resistance of the titanium silicide films is abruptly increased. Fig. 52 shows exemplary gate dependency of gate resistance in titanium silicide TiSi_2 .

SUMMARY OF THE INVENTION

According to a first aspect of the present invention, a method of fabricating a MIS transistor includes a gate electrode forming step of forming a gate electrode containing polycrystalline silicon which is opposed to a silicon substrate through a gate insulating film, a side wall forming step of forming side walls on both sides of the gate electrode, and a silicide step of forming desired silicide films on upper portions of the gate electrode and a source/drain layer, and the side wall forming step has steps of depositing a first insulating film on a region including at least one of the both sides of the gate electrode and a surface of the silicon substrate which is allowed to be exposed by the gate electrode and in contact with the at least one of said both sides, depositing a second insulating film which is opposed to the at least one of said both sides and the surface through the first insulating film, and etching back the first and second insulating films thereby forming the at least one of the both sides walls of a two-layer structure, and the method further includes an etching step of etching the first insulating film in a larger amount than the second insulating film before the silicide step.

According to a second aspect of the present invention, compositions of the first and second insulating films are different from each other, and the etching step is adapted to isotropically etch the first insulating film.

According to a third aspect of the present invention, compositions of the first

and second insulating films are different from each other, and the etching step is adapted to etch the first insulating film through anisotropic etching at a higher etching rate in a vertical direction which is perpendicular to the silicon substrate as compared with an etching rate in a horizontal width direction.

5 According to a fourth aspect of the present invention, the method further includes a step of roughening an upper surface of the gate electrode before the salicide step.

10 The present invention is also directed to a MIS transistor. According to a fifth aspect of the present invention, a MIS transistor includes a gate electrode which is formed to be opposed to a silicon substrate through a gate insulating film and has a silicified upper portion, and side walls which are formed on the silicon substrate on both sides of the gate electrode and have grooves adjacent to the gate electrode, and the gate electrode is silicified up to walls of the gate electrode in the grooves.

15 According to a sixth aspect of the present invention, the side walls have cavities exposing a source/drain layer which is formed on the silicon substrate.

 According to a seventh aspect of the present invention a surface of the gate electrode is roughened.

20 According to an eighth aspect of the present invention, a MIS transistor includes a gate electrode which is formed to be opposed to a silicon substrate through a gate insulating film and has a silicified upper portion, and side walls which are formed on the silicon substrate on both sides of the gate electrode so that the side walls are higher than the gate electrode, and the side walls are provided with silicon films on walls closer to the gate electrode to be connected with the gate electrode, while a surface of the gate electrode is silicified up to surfaces of
25 the silicon films.

According to a ninth aspect of the present invention, both of the surfaces of the gate electrode and the silicon films are roughened.

According to a tenth aspect of the present invention, a MIS transistor includes a gate electrode which is formed to be opposed to a silicon substrate through a gate insulating film and has a silicified upper portion, and side walls having L-shaped sections which are formed on the silicon substrate on both sides of the gate electrode so that the side walls are higher than the gate electrode.

According to an eleventh aspect of the present invention, a surface of the gate electrode is roughened.

In the method of fabricating a MIS transistor according to the first aspect of the present invention, the grooves can be formed in the side walls of the two-layer structure before the silicide step for increasing the distance between the surfaces of the gate electrode and the source/drain layer, whereby it is possible to effectively prevent short-circuiting across the gate electrode and the source/drain layer caused by silicide creeping along the surfaces of the side walls in formation of the silicide films. Further, the exposed portion of the gate electrode or the source/drain layer is increased due to the grooves formed in the side walls and the width of the silicide film formed on the gate electrode or the source/drain layer can be substantially increased, whereby phase transition of silicide is effectively simplified for reducing gate resistance.

In the method of fabricating a MIS transistor according to the second aspect of the present invention, both of the grooves adjacent to the gate electrode and those (cavities) adjacent to the silicon substrate can be simultaneously formed before the silicide step for improving the effect of preventing short-circuiting caused by silicide creeping along the side wall surfaces, and an effect of readily

causing phase transition and reducing resistance can be attained by both silicide films provided on the gate electrode and the source/drain layer.

In the method of fabricating a MIS transistor according to the third aspect of the present invention, the grooves adjacent to the gate electrode can be formed in the side walls by anisotropic etching before the silicide step while no grooves are formed in portions of the side walls which are in contact with the silicon substrate, whereby the grooves can be simply formed when no grooves are to be formed in the portions which are in contact with the silicon substrate.

In the method of fabricating a MIS transistor according to the fourth aspect of the present invention, the surface of the gate electrode is roughened before the silicide step so that the effective width of the silicide film can be further increased, whereby phase transition can be further effectively simplified for reducing the resistance.

In the MIS transistor according to the fifth aspect of the present invention, the exposed portion of the gate electrode surface is increased by the grooves adjacent to the gate electrode, whereby phase transition of silicide is simplified in silicification of the gate electrode surface, and hence increase of gate resistance can be suppressed and the gate electrode can be effectively refined without reducing the operating speed of the MIS transistor.

In the MIS transistor according to the sixth aspect of the present invention, the exposed area of the source/drain layer is increased by the cavities formed in the side walls to attain an action substantially identical to increase of the source/drain layer for the silicide film formed thereon, whereby phase transition of silicide is simplified and resistance parasitic to the source/drain layer can be effectively reduced.

In the MIS transistor according to the seventh aspect of the present invention, the surface of the gate electrode is roughened and this roughening substantially serves as increase of the width of the silicide film formed on the gate electrode surface, phase transition of silicide can be simplified and increase of gate resistance
5 can be suppressed also in case of further refinement, and the refinable range is effectively widened without reducing the operating speed of the MIS transistor.

In the MIS transistor according to the eighth aspect of the present invention, the silicon films formed on the walls of the side walls are connected with the gate electrode while the both are silicified, whereby this substantially serves as increase
10 of the width of the silicide film formed on the gate electrode surface by the silicon films formed on the inner walls, phase transition of silicide can be simplified and increase of gate resistance can be suppressed in case of refining the gate electrode, and the refinable range is effectively widened without reducing the operating speed of the MIS transistor.

In the MIS transistor according to the ninth aspect of the present invention, the surface of the gate electrode is roughened, whereby this substantially serves as increase of the width of the silicide film formed on the gate electrode surface, phase
15 transition of silicide can be simplified and increase of gate resistance can be suppressed also in case of further refinement, and the refinable range is effectively widened without reducing the operating speed of the MIS transistor.
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In the MIS transistor according to the tenth aspect of the present invention, the side walls having L-shaped sections are formed to be higher than the gate electrode, whereby the action of preventing short-circuiting across the gate electrode and the source/drain layer can be effectively improved.

25 In the MIS transistor according to the eleventh aspect of the present invention,

the surface of the gate electrode is roughened, whereby this substantially serves as increase of the width of the silicide film formed on the gate electrode surface, phase transition of silicide can be simplified and increase of gate resistance can be suppressed also in case of further refinement, and the refinable range is effectively widened without reducing the operating speed of the MIS transistor.

An object of the present invention is to provide a technique of avoiding short-circuiting across a gate electrode and a source/drain layer in formation of silicide films. Another object of the present invention is to provide a technique of obtaining silicide films whose sheet resistance is not increased even if the width of silicified parts such as upper portions of a gate electrode and a source/drain layer is small.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 - Fig. 5 are sectional views showing steps of fabricating a MOS transistor according to an embodiment 1 of the present invention;

Fig. 6 - Fig. 8 are sectional views showing steps of fabricating a MOS transistor according to an embodiment 2 of the present invention;

Fig. 9 - Fig. 13 are sectional views showing steps of fabricating a first MOS transistor according to an embodiment 3 of the present invention;

Fig. 14 - Fig. 16 are sectional views showing steps of fabricating a second MOS transistor according to the embodiment 3 of the present invention;

Fig. 17 and Fig. 18 are sectional views showing steps of fabricating a third

MOS transistor according to the embodiment 3 of the present invention;

Fig. 19 and Fig. 20 are sectional views showing steps of fabricating a first MOS transistor according to an embodiment 4 of the present invention;

Fig. 21 and Fig. 22 are sectional views showing steps of fabricating a second MOS transistor according to the embodiment 4 of the present invention;

Fig. 23 and Fig. 24 are sectional views showing steps of fabricating a third MOS transistor according to the embodiment 4 of the present invention;

Fig. 25 – Fig. 29 are sectional views showing steps of fabricating a MOS transistor according to an embodiment 5 of the present invention;

Fig. 30 – Fig. 34 are sectional views showing steps of fabricating a first MOS transistor according to an embodiment 6 of the present invention;

Fig. 35 and Fig. 36 are sectional views showing steps of fabricating a second MOS transistor according to the embodiment 6 of the present invention;

Fig. 37 and Fig. 38 are sectional views showing steps of fabricating a third MOS transistor according to the embodiment 6 of the present invention;

Fig. 39 – Fig. 42 are sectional views showing steps of fabricating a first MOS transistor according to an embodiment 7 of the present invention;

Fig. 43 – Fig. 46 are sectional views showing steps of fabricating a second MOS transistor according to an embodiment 7 of the present invention;

Fig. 47 – Fig. 50 are sectional views showing steps of fabricating a conventional MOS transistor;

Fig. 51 is a sectional view showing a part of Fig. 50 in an enlarged manner;
and

Fig. 52 is a graph showing the relation between gate lengths and gate resistance in a gate electrode made of titanium silicide.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment 1.

A MOS transistor and a method of fabricating the same according to an embodiment 1 of the present invention are described with reference to Figs. 1 to 5. Figs. 1 to 5 are sectional views showing a silicon substrate 1 to be formed with a MOS transistor, particularly a MOS field-effect transistor (hereinafter referred to as a MOSFET) in respective fabrication steps according to the embodiment 1 of the present invention.

First, a general method of fabricating a MOSFET is employed for forming isolation oxide films 2, a well 1a and an impurity layer 3 for controlling a threshold voltage are formed on a portion of the silicon substrate 1 to be formed with the MOSFET. Further, an oxide film (gate insulating film 4) of about 6.5 nm in thickness, for example, is formed on a region enclosed with the isolation oxide films 2 by the general fabrication method, and a polycrystalline silicon film for forming a gate electrode is deposited on this oxide film in a thickness of about 200 nm, for example. After gate doping is performed, a resist film is formed and patterned, for anisotropically etching the polycrystalline silicon film thereby forming a gate electrode 5 (see Fig. 1).

Then, nitrogen is injected into the overall surfaces of regions exposing silicon, and thereafter LDD layers 6 are formed. Silicon oxide is deposited by CVD on the overall surface as a first insulating film of about 15 to 500 Å (e.g., about 150 Å) for forming a silicon oxide film 11, and thereafter silicon nitride is deposited by CVD as a second insulating film of about 300 to 1000 Å (e.g., about 800 Å) for forming a silicon nitride film 12 (see Fig. 2).

Then, the silicon nitride film 12 and the silicon oxide film 11 are etched back

by RIE, for forming side walls 15. The side walls 15, having a two-layer structure, consist of a buffer layer 13 which is formed to be in contact with the silicon substrate 1, and silicon nitride layers 14 formed on this buffer layer 13.

5 An impurity is added to regions to be formed with source/drain layers and thereafter RTA is carried out at a temperature of about 1000°C for 30 seconds, for forming high-concentration source/drain layers 8, as shown in Fig. 3.

10 Then, the buffer layer 13 forming the upper portions of the side walls 15 is anisotropically etched with gas 16 hardly corroding the polycrystalline silicon film on the gate electrode 5 and the silicon nitride film 12 serving as the second insulating film, or etched by vapor-phase hydrofluoric acid treatment with sufficient anisotropy. At this time, the buffer layer 13 is etched up to a vertical intermediate portion of the gate electrode 5, not to expose the silicon substrate 1. Thus, grooves 17 can be formed in regions of the side walls 15 adjacent to the gate electrode 5, as shown in Fig. 4.

15 Then, silicide films 18 are formed on an upper portion of the gate electrode 5 and its surfaces which are in contact with the grooves 17 as well as upper portions of the high-concentration source/drain layers 8 respectively through a conventional silicide step, as shown in Fig. 5.

20 The MOS transistor is fabricated through the aforementioned steps, whereby the silicide film 18 formed on the gate electrode 5, which has grown to creep along side surfaces of the side walls 15, can be stopped in the grooves 17, for example, to be prevented from creeping along the side surfaces of the side walls 15. Thus, short-circuiting across the gate electrode 5 and the high-concentration source/drain layers 8 can be effectively suppressed as compared with the prior art. From another
25 point of view, the distances between the gate electrode 5 and the high-

concentration source/drain layers 8 along the surfaces of the side walls 15 are substantially increased by the grooves 17.

In the MOS transistor having the grooves 17, further, the silicide films 18 can grow also on surfaces of the gate electrode 5 located in the grooves 17 respectively.

Thus, the width of the silicide film 18 formed on the gate electrode 5 is substantially increased, whereby phase transition of the crystal structure of silicide from a C49 phase to a C54 phase can readily take place in case of titanium silicide, for example, and the gate resistance can be reduced by effectively increasing the width of the silicide film 18 to be at least $0.5\ \mu\text{m}$ in case of forming the gate electrode 5 having a short gate length. The parasitic resistance of the device can be remarkably reduced due to such reduction of the gate resistance, for enabling the MOS transistor to operate at a high speed.

When the gate length is $0.35\ \mu\text{m}$, for example, the length of the silicified surfaces is $(0.35 + 0.1 \times 2)\ \mu\text{m}$ assuming that the depth D1 of the grooves 17 shown in Fig. 4 is $0.1\ \mu\text{m}$, and the width of the silicide film 18 exceeds $0.5\ \mu\text{m}$, whereby the gate resistance can be remarkably reduced, as understood also from Fig. 52.

While the side walls 15 have a two-layer structure formed by the buffer layer 13 consisting of silicon oxide and the silicon nitride layers 14, the materials for the side walls 15 are not restricted to silicon oxide and silicon nitride, but outer sides and inner sides, which are closer to the gate electrode 5, of the side walls 15 may alternatively be formed by second and first insulating films which are hardly and readily corroded by an etchant not corroding the gate electrode 5 respectively, in order to attain the effect of the present invention.

Embodiment 2.

A MOS transistor and a method of fabricating the same according to an embodiment 2 of the present invention are described with reference to Figs. 6 to 8. Figs. 6 to 8 are sectional views showing steps of fabricating the MOS transistor according to the embodiment 2 of the present invention respectively.

5 First, side walls 15 having a two-layer structure and a gate electrode 5 are formed on a region of a silicon substrate 1 enclosed with isolation oxide films 2 as shown in Fig. 6, by the same method as that shown in relation to the embodiment 1 of the present invention.

10 Then, a buffer layer 13 is isotropically etched with a hydrofluoric acid solution 20 hardly corroding polycrystalline silicon and silicon nitride while anisotropically corroding silicon oxide, for forming grooves 17 and cavities 19 in the side walls 15, as shown in Fig. 7. At this time, the etching rate and the etching time are so set that the etching is ended on a vertical intermediate portion of the gate electrode 5 before the grooves 17 reach surface portions of the silicon substrate 1 located on both sides of the gate electrode 5 due to excessive corrosion of portions of the buffer layer 13 located on side surfaces of the gate electrode 5 respectively. Further, the etching rate and the etching time are so set that the etching is ended on an intermediate portion of the side wall width W before the cavities 19 reach the gate electrode 5 due to excessive corrosion of the buffer layer 13 forming lower portions of the side walls 15.

20 Then, silicide films 21 are formed on an upper portion of the gate electrode 5 and its side surfaces facing the grooves 17 as well as upper portions of high-concentration source/drain layers 8 respectively by a conventional silicide step. The upper portions of the high-concentration source/drain layers 8 include portions exposed by the cavities 19.

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Due to fabrication of the MOS transistor through the aforementioned steps, the creeping distance of silicide can be effectively increased by the grooves 17 similarly to the fabrication method for the MOS transistor according to the embodiment 1 of the present invention, while the silicide films 21 formed on the surfaces of the high-concentration source/drain layers 8 can be prevented from creeping up. For example, the creeping distance of silicide along the surfaces of the side walls 15 is increased by the lengths of the cavities 19, whereby the silicide films 21 formed on the surfaces of the high-concentration source/drain layers 8 can be prevented from further extension by the cavities 19.

Further, the MOS transistor provided with the grooves 17 has an effect of reducing the gate length without increasing the resistance value of the gate electrode 5, similarly to the embodiment 1 of the present invention. In the MOS transistor according to the embodiment 2 of the present invention having the cavities 19, in addition, the silicide films 21 can also grow on the surfaces of the high-concentration source/drain layers 8 in the cavities 19. For the silicide films 21 formed on the surfaces of the high-concentration source/drain layers 8, therefore, the MOS transistor has such an effect that the widths of the high-concentration source/drain layers 8, i.e., the distances between the side walls 15 and the isolation oxide films 2, are substantially increased. In case of forming a MOS transistor having short distances between the isolation oxide films 2 and the side walls 15, phase transition from a C49 phase to a C54 phase readily takes when the length of the high-concentration source/drain layers 8 is rendered substantially in excess of $0.5\ \mu\text{m}$ by the depth of the cavities 19 in case of titanium silicide, for example, whereby the parasitic resistance of the source/drain layers 8 can be reduced. Due to such reduction of the parasitic resistance of the source/drain layers

8, the MOS transistor can operate at a higher speed as compared with the conventional MOS transistor of the same size.

Embodiment 3.

A MOS transistor and a method of fabricating the same according to an
5 embodiment 3 of the present invention are described with reference to Figs. 9 to 14. Figs. 9 to 14 are sectional views showing steps of fabricating the MOS transistor according to the embodiment 3 of the present invention respectively.

First, isolation oxide films 2, a well 1a and an impurity layer 3 for controlling
10 a threshold voltage are formed on a silicon substrate 1 by a general method of fabricating a MOSFET. Then, a gate insulating film 4 is deposited on the silicon substrate 1, and an amorphous silicon film 30 is further deposited thereon. Fig. 9 is a sectional view showing the silicon substrate 1 on which the amorphous silicon film 30 is deposited. This amorphous silicon film 30 is deposited at an evaporation temperature of about 520°C under evaporation pressure of about 2 Torr, with silane
15 (SiH_4) at a flow rate of 1300 sccm or disilane (Si_2H_6) at a flow rate of 100 sccm. At this time, carrier gas such as any of nitrogen (N_2), hydrogen (H_2), helium (He) and the like, for example, is fed by about 500 sccm. However, the amorphous silicon film 30 can be formed without feeding such carrier gas.

Then, disilane is adsorbed on a silicon surface in a molecular state and
20 decomposed on the surface, thereby forming nuclei for polycrystalline silicon. Then, the temperature of the silicon substrate 1 is increased to about 600 to 700°C for making crystal growth from the nuclei for polycrystalline silicon on the amorphous silicon 30, thereby converting amorphous silicon to polycrystalline silicon. Thus formed is a silicon film 31 including a surface roughened by a
25 number of semispherical projections 32, as shown in Fig. 10. In case of forming

a TiSi_2 film of 300 to 1000 Å in thickness, the diameters of the projections 32 are preferably at least $0.05\ \mu\text{m}$, in order to sufficiently attain an effect of simplifying phase transition. If the physical gate length is 0.3 to $0.5\ \mu\text{m}$, the diameters of the projections 32 are preferably not more than about $0.3\ \mu\text{m}$, in order to suppress dispersion of the substantial gate length when a plurality of sections are observed perpendicularly to the plane of the figure. In general, the sizes, i.e., the diameters of the semispherical projections 32 can be measured by observation with a scanning microscope. Roughening treatment is described in "Growth mechanism of polycrystalline Si films with hemispherical grains" by Toru Tatsumi, Akira Sakai, Taeko Ikarashi and Hirohito Watanabe, Applied Physics, 1992, Vol. 61, No. 11, pp. 1147 to 1151, for example.

Then, the silicon film 31 is patterned to form a gate electrode 5, followed by formation of LDD layers 6. Thereafter a silicon oxide film is deposited by CVD as a first insulating film of about 150 to 500 Å, for example, and a silicon nitride film is deposited on this first insulating film by CVD as a second insulating film of about 300 to 1000 Å, for example. The first and second insulating films are etched back by RIE, whereby side walls 15 of a two-layer structure can be formed on both sides of the gate electrode 5, as shown in Fig. 11. These side walls 15 are formed by a buffer layer 13, having L-shaped sections and consisting of the first insulating film, which is in contact with the silicon substrate 1 and the gate electrode 5, and silicon nitride layers 14, consisting of the second insulating film, which are formed to be held by two sides of the buffer layer 13 defining the L-shaped sections.

Thereafter grooves 17 are formed in the side walls 15 to be adjacent to an upper portion of the gate electrode 5 by a method similar to that in the embodiment

1 of the present invention, as shown in Fig. 12. High-concentration source/drain layers 8 are formed, and thereafter silicide films 33 are formed on upper portions of the gate electrode 5 and the high-concentration source/drains 8 by a salicide step similarly to the embodiment 1 of the present invention, as shown in Fig. 13.

5 The silicide films 33 according to the embodiment 3 are different from the silicide films 18 according to the embodiment 1 in a point that the upper surface of the gate electrode 5 is roughened by the projections 32 in the embodiment 3. When the MOS transistors according to the embodiments 1 and 3 are rendered identical in size to each other, therefore, the substantial width of the silicide film
10 33 formed on the gate electrode 5 according to the embodiment 3 is longer than that in the embodiment 1. Thus, the gate length remarkably increasing the gate resistance by phase transition of silicide is smaller in the MOS transistor according to the embodiment 3 as compared with that according to the embodiment 1. Therefore, the MOS transistor according to the embodiment 3 is further suitable for
15 refinement, and has a higher effect of improving the degree of integration when applied to an integrated circuit.

 The roughening step in the embodiment 3 of the present invention may alternatively be carried out after forming the gate electrode 5 consisting of amorphous silicon by patterning the amorphous silicon film 30. Fig. 14 shows the
20 roughened state of the gate electrode 5. In this case, the remaining steps are similar to those described with reference to the embodiment 3. Figs. 15 and 16 are sectional views showing the silicon substrate 1 immediately after formation of the side walls 15 and after formation of the silicide films 33 respectively.

 Further alternatively, the gate electrode 5 prepared from amorphous silicon
25 may be roughened after formation of the side walls 15. In this case, however, it

is necessary to employ CVD as the method of depositing the first and second insulating films for forming the side walls 15 while keeping the temperatures for depositing the first and second insulating films at levels of not more than 600°C, so that the material forming the gate electrode 5 is not converted from amorphous silicon to polycrystalline silicon. The buffer layer 13 presents the sectional shapes shown in Fig. 4 when anisotropically etched, and the gate electrode 5 consists of amorphous silicon at this time. Fig. 17 shows a sectional shape of the silicon substrate 1 after roughening the gate electrode 5 having the sectional shape shown in Fig. 4. Fig. 18 shows a state of the silicon substrate 1, having the shape shown in Fig. 17, subjected to a salicide step for forming the silicide films 33 on the surfaces of the gate electrode 5 and the high-concentration source/drain layers 8 respectively.

Embodiment 4.

A MOS transistor and a method of fabricating the same according to an embodiment 4 of the present invention are described with reference to Figs. 10, 19 and 20. Figs. 19 and 20 are sectional views showing steps of fabricating the MOS transistor according to the embodiment 4 of the present invention respectively.

First, a roughened polycrystalline silicon film 31 is formed by a method similar to that in the embodiment 3 of the present invention, as shown in Fig. 10.

Then, a roughened gate electrode 5 and side walls 15 having grooves 17 and cavities 19 are formed by a method similar to that described with reference to the embodiment 2 of the present invention, as shown in Fig. 19. High-concentration source/drain layers 8 are formed on the silicon substrate 1 shown in Fig. 19, and thereafter a salicide step is applied to the silicon substrate 1, thereby forming silicide films 33 on a surface of the gate electrode 5 and upper surfaces of the

high-concentration source/drain layers 8 respectively (see Fig. 20).

The roughening step in the embodiment 4 of the present invention may alternatively be carried out after forming the gate electrode 5 by patterning the amorphous silicon film 30. Fig. 14 shows the roughened state of the gate electrode 5. In this case, the remaining steps are similar to those described with reference to the embodiment 4 of the present invention. Figs. 21 and 22 are sectional views showing the silicon substrate 1 immediately after formation of the side walls 15 and after formation of the silicide films 33 respectively.

Further alternatively, the gate electrode 5 prepared from amorphous silicon may be roughened after formation of the side walls 15. In this case, however, it is necessary to employ CVD as the method of depositing the first and second insulating films for forming the side walls 15 while keeping the temperatures for depositing the first and second insulating films at levels of not more than 600°C, so that the material forming the gate electrode 5 is not converted from amorphous silicon to polycrystalline silicon. A buffer layer 13 presents sectional shapes shown in Fig. 7 when anisotropically etched, and the gate electrode 5 consists of amorphous silicon at this time. Fig. 23 shows a sectional shape of the silicon substrate 1 after roughening the gate electrode 5 having the sectional shape shown in Fig. 7. Fig. 24 shows a state of the silicon substrate 1, having the shape shown in Fig. 23, formed with the high-concentration source/drain layers 8 and subjected to a silicide step for forming the silicide films 33 on the upper surfaces of the gate electrode 5 and the high-concentration source/drain layers 8 respectively.

Embodiment 5

A MOS transistor and a method of fabricating the same according to an embodiment 5 of the present invention are described with reference to Figs. 25 to

29. Figs. 25 to 29 are sectional views showing steps of fabricating the MOS transistor according to the embodiment 5 of the present invention respectively.

First, isolation oxide films 2, a well 1a and an impurity layer 3 for controlling a threshold voltage are formed on a silicon substrate 1 by a general method of fabricating a MOSFET. Then, a gate insulating film 4 is deposited on the silicon substrate 1, and a polycrystalline silicon film for defining a gate electrode is deposited thereon.

Then, a stacked film is deposited on the polycrystalline silicon film by about 500 Å, for example. This stacked film is prepared from silicon nitride, for example. A resist film is patterned through a photolithographic step, thereafter the stacked film is anisotropically etched, and the polycrystalline silicon film is anisotropically etched through the etched stacked film serving as a mask, thereby forming a gate electrode 5. At this time, a cap layer 40 is formed on the gate electrode 5, as shown in Fig. 25.

After formation of LDD layers 6, a silicon oxide film is deposited by CVD as an insulating film of about 600 to 1500 Å, for example, for forming side walls. The silicon oxide film is etched back by RIE for forming side walls 41, as shown in Fig. 26. At this time, the etching conditions are so set that the cap layer 40 prepared from silicon nitride still remains after the silicon oxide film is etched back.

Then, silicon nitride is etched with hot phosphoric acid hardly corroding polycrystalline silicon and silicon oxide, for removing the cap layer 40. The side walls 41 formed in this manner are higher than the gate electrode 5.

Then, polycrystalline silicon is deposited by about 300 to 500 Å, for forming a polycrystalline silicon (or amorphous silicon) layer 43. Fig. 27 is a sectional view showing this state. This polycrystalline silicon (or amorphous silicon) layer

43 is etched back for forming side walls 44 of polycrystalline silicon (or amorphous silicon) on inner walls of the side walls 41, as shown in Fig. 28. At this time, the gate electrode 5 may be slightly etched, so far as the same does not reach the gate insulating film 4. Further, the silicon substrate 1 may also be etched by a depth of not more than about 500 Å, for example, not influencing the transistor properties.

Then, high-concentration source/drain layers 8 are formed. Thereafter silicide films 45 are formed on surfaces of the gate electrode 5 and the high-concentration source/drain layers 8 respectively through a silicide step similar to that of the prior art, as shown in Fig. 29.

The MOS transistor formed in the aforementioned manner has the high side walls 41, whereby the distances between the side walls 44 which are electrically connected with the gate electrode 5 and the high-concentration source/drains 8 are longer as compared with side walls of general height, and it is possible to suppress occurrence of short-circuiting across the gate electrode 5 and the source/drain layers 8 caused by the silicide films 45 creeping along surfaces of the side walls 41.

Further, the silicide films 45 are formed also on the surfaces of the side walls 44 of polycrystalline silicon formed on the inner walls of the side walls 41, whereby this serves as increase of the widths of the silicide films 45. In case of refining the gate electrode 5 to a gate length hardly causing phase transition of silicide, it is possible to readily cause phase transition of the silicide films 45 by extending the gate length by the lengths of the side walls 44 with respect to the silicide films 45. The gate resistance can be reduced, whereby the parasitic resistance of the MOS transistor can be extremely reduced as compared with a conventional MOS transistor of the same size, and the inventive MOS transistor can

operate at a higher speed.

While silicon nitride is employed for the cap layer 40 in the aforementioned embodiment, the cap layer 40 may be prepared from any material which can etch the silicon substrate 1 with sufficient selectivity for the side walls 41 and the gate electrode 5.

Embodiment 6.

A MOS transistor and a method of fabricating the same according to an embodiment 6 of the present invention are described with reference to Figs. 30 to 34. Figs. 30 to 34 are sectional views showing steps of fabricating the MOS transistor according to the embodiment 6 of the present invention respectively.

First, a silicon substrate 1 is so prepared that a polycrystalline silicon film 31 having an irregular surface as shown in Fig. 10 is deposited thereon, similarly to the fabrication method according to the embodiment 3 of the present invention.

Then, a stacked film is deposited on the polycrystalline silicon film 31 by about 500 Å, for example. This stacked film is prepared from silicon nitride, for example. A resist film is patterned through a photolithographic step, thereafter the stacked film is anisotropically etched, and the polycrystalline silicon film 31 is anisotropically etched through the etched stacked film serving as a mask, thereby forming a gate electrode 5. At this time, a cap layer 40 having an irregular surface is formed on the gate electrode 5, as shown in Fig. 30.

Sectional shapes shown in Figs. 31 to 34 are formed through steps identical to those for working the silicon substrate 1 shown in Figs. 26 to 29 in relation to the embodiment 5 of the present invention.

In order to fabricate the MOS transistor according to the embodiment 6 of the present invention, a step for roughening a surface of the gate electrode 5 must be

added to the steps similar to those for fabricating the MOS transistor according to the embodiment 5 of the present invention.

In the MOS transistor according to the embodiment 6 of the present invention, roughening of the surface of the gate electrode 5 has the same effect as that the widths of silicide films 45 are substantially increased as compared with the MOS transistor according to the embodiment 5. When the gate electrode 5 is refined to a gate length hardly causing phase transition of silicide, therefore, the gate resistance can be reduced by facilitating phase transition of the silicide films 45, and hence the MOS transistor according to the embodiment 6 of the present invention is suitable for refinement as compared with that according to the embodiment 5.

Among the fabrication steps in the embodiment 6 of the present invention, the step of roughening the surface of the gate electrode 5 may be carried out before formation of side walls 41 and immediately after formation of the gate electrode 5. Figs. 35 and 36 corresponding to Figs. 28 and 29 respectively show the sectional shape of a silicon substrate 1 which is thereafter formed through steps similar to those of the embodiment 6.

Among the fabrication steps of the embodiment 6 of the present invention, the step of roughening the surface of the gate electrode 5 may alternatively be carried out after formation of side walls 41 before forming polycrystalline silicon or amorphous silicon layers on inner walls of the side walls 41. In this case, it is necessary to deposit silicon nitride through a CVD process at a low temperature of not more than 600°C, for preventing polycrystal growth of amorphous silicon forming the gate electrode 5 in deposition of silicon oxide for forming the side walls 41.

Among the fabrication steps of the embodiment 6 of the present invention, the step of roughening the surface of the gate electrode 5 may further alternatively be carried out after a step of forming side walls 44 of silicon on inner walls of side walls 41. Figs. 37 and 38 corresponding to Figs. 28 and 29 respectively illustrate a sectional shape of a silicon substrate 1 thereafter formed through steps similar to those of the embodiment 6. Also in this case, it is necessary to deposit silicon oxide for forming the side walls 41 through a CVD process at a low temperature of not more than 600°C.

Embodiment 7.

A MOS transistor and a method of fabricating the same according to an embodiment 7 of the present invention are described with reference to Figs. 25 and 39 to 42. Figs. 39 to 42 are sectional views showing steps of fabricating the MOS transistor according to the embodiment 7 of the present invention respectively.

First, a silicon substrate 1 is so prepared that a cap layer 40 is formed on a gate electrode 5 as shown in Fig. 25 through steps similar to those of the embodiment 5 of the present invention.

Then, after forming LDD layers 6, silicon oxide is deposited by CVD as a first insulating film of about 150 to 500 Å for forming side walls, and silicon nitride is deposited on this silicon oxide film as a second insulating film of about 300 to 1000 Å for forming side walls. Fig. 39 shows the first and second insulating films etched back by RIE. At this time, conditions are so set that the cap layer 40 provided on the gate electrode 5 still remains after the first and second insulating films are etched back. Side walls 50 of a two-layer structure shown in Fig. 39 are formed by first and second insulating films 51 and 52.

Then, silicon nitride is isotropically etched by hot phosphoric acid 53, as

shown in Fig. 40. The cap layer 40 provided on the gate electrode 5 and the second insulating films 52 are removed by this etching. Thus formed are side walls 55 having L-shaped sections which are higher than the gate electrode 5, as shown in Fig. 41.

5 Then, high-concentration source/drain layers 8 are formed through the side walls 55 serving as masks, and thereafter silicide films 56 are formed on surfaces of the gate electrode 5 and the high-concentration source/drains 8 respectively through a conventional silicide step. Fig. 42 shows a sectional shape of the silicon substrate 1 after formation of the silicide films 56.

10 In the fabrication steps for the MOS transistor according to the embodiment 7 of the present invention, the side walls 55 having L-shaped sections which are higher than the gate electrode 5 are formed before the silicide step, whereby the surface distances of the side walls 55 between the gate electrode 5 and the high-concentration source/drain layers 8 are longer as compared with the side walls of
15 the MOS transistor according to the aforementioned respective embodiments, and hence short-circuiting hardly takes place across the gate electrode 5 and the high-concentration source/drain layers 8.

In the embodiment 7 of the present invention, a step of roughening the surface of the gate electrode 5 can be added for forming a MOS transistor provided with
20 high side walls having L-shaped sections and the roughened gate electrode 5. In this case, a silicon substrate 1 having a roughened polycrystalline silicon film 31 shown in Fig. 10 is prepared, so that the fabrication method of the embodiment 7 is thereafter applied. In this case, sectional shapes shown in Figs. 43 to 46, for example, appear in the respective steps shown in Figs. 39 to 42 in relation to the
25 embodiment 7. Also in this case, an effect of reducing gate resistance is attained

by simplification of phase transition of silicon. Thus, the MOS transistor obtained by roughening the surface of the gate electrode 5 in the embodiment 7 is suitable for refinement as compared with the MOS transistor having the unroughened gate electrode 5, similarly to that the MOS transistor according to the embodiment 6 is suitable for refinement as compared with that according to the embodiment 5.

While crystal growth is employed for roughening in each of the aforementioned embodiments, heterogeneous corrosion such as wet treatment employing hot phosphoric acid, for example, may alternatively be employed for the roughening. In this case, polycrystalline silicon is subjected to roughening by hot phosphoric acid under such conditions that silicon is dissolved in the hot phosphoric acid in a concentration not more than a saturation concentration, the temperature is 130 to 160°C, and about 70 to 90 % of hot phosphoric acid is employed.

While the structure according to the present invention is provided on both sides of the side walls in each of the aforementioned embodiments, the effect of the present invention can be attained also when the inventive structure is provided only on either one of the side walls, as a matter of course.

While the invention has been shown and described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications and variations can be devised without departing from the scope of the invention.